Docket No.: YOR920030530US1
CBLH/20140-00316-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Katherine L. Saenger et al.

Application No.: Not Yet Assigned | Confirmation No.:

Filed: Concurrently Herewith | Art Unit: N/A

For: FIELD EFFECT TRANSISTOR WITH ETCHED-BACK GATE DIELECTRIC | Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A copy of each reference on the PTO/SB/08 is attached.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this

application by this firm) to our Deposit Account No. 50-0510, under Order No. 20140-00316-US. A duplicate copy of this paper is enclosed.

Dated: 12/10/03

Respectfully submitted,

By _____

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PTO/SB/08a/b (06-03)
Approved for use through 07/31/2003. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	Concurrently Herewith
First Named Inventor	Katherine L. Saenger et al.
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	YOR920030530US1 CBLH/20140-00316-US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	JAKUB KEDZIERSKI, et al., Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation, IBM Semiconductor Research and Development Center pgs. 247-250	
	CB	B. GUILLAUMOT, et al., 75nm Damascene Metal Gate and High-k Integration for Advanced CMOS Devices, Cedex France, Meylan France, Marseille France, pgs. 355-358	
	CC	KATHERINE L. SAENGER, et al., A Selective Etching Process for Chemically Inert High-k Oxides, Mat. Res. Soc. Symp. Proc. Vol. 745© 2003 Material Research Society, IBM Research Division, T.J. Watson Research Center	
	CD	MATSUO J. YAMADA, , et al., Surface processing by gas cluster ion beams at the atomic (molecular) level, Ion Beam Engineering Experimental Laboratory, Kyoto University, Sakyo, Kyoto 606, Japan	

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